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C

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A

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D

Revision History

0.1 - Initial pre-release
0.2 - Checked by DAB, FJ, JG. Fixed minor mistakes.
0.3 - Removed optic fiber components due to lack of space on the board, added UMAC variant to build list, filled in refdes for build variants

1.0 - Board rev 1. Includes microwave switch assembly components, DAC SHDN pin tied to +5V instead of GND

1.1 - Change FB8-11 to use component MZA3216Y102B instead of DLP31

Build Variants

UMAC chassis compatible

NOUMAC - No UMAC compatibility

Do not populate:
P1

UMAC - Draw power from UMAC

Do not populate:
FL1, F13, D28, U27, C46

Parallel I/O

NOPAR - No Parallel I/O

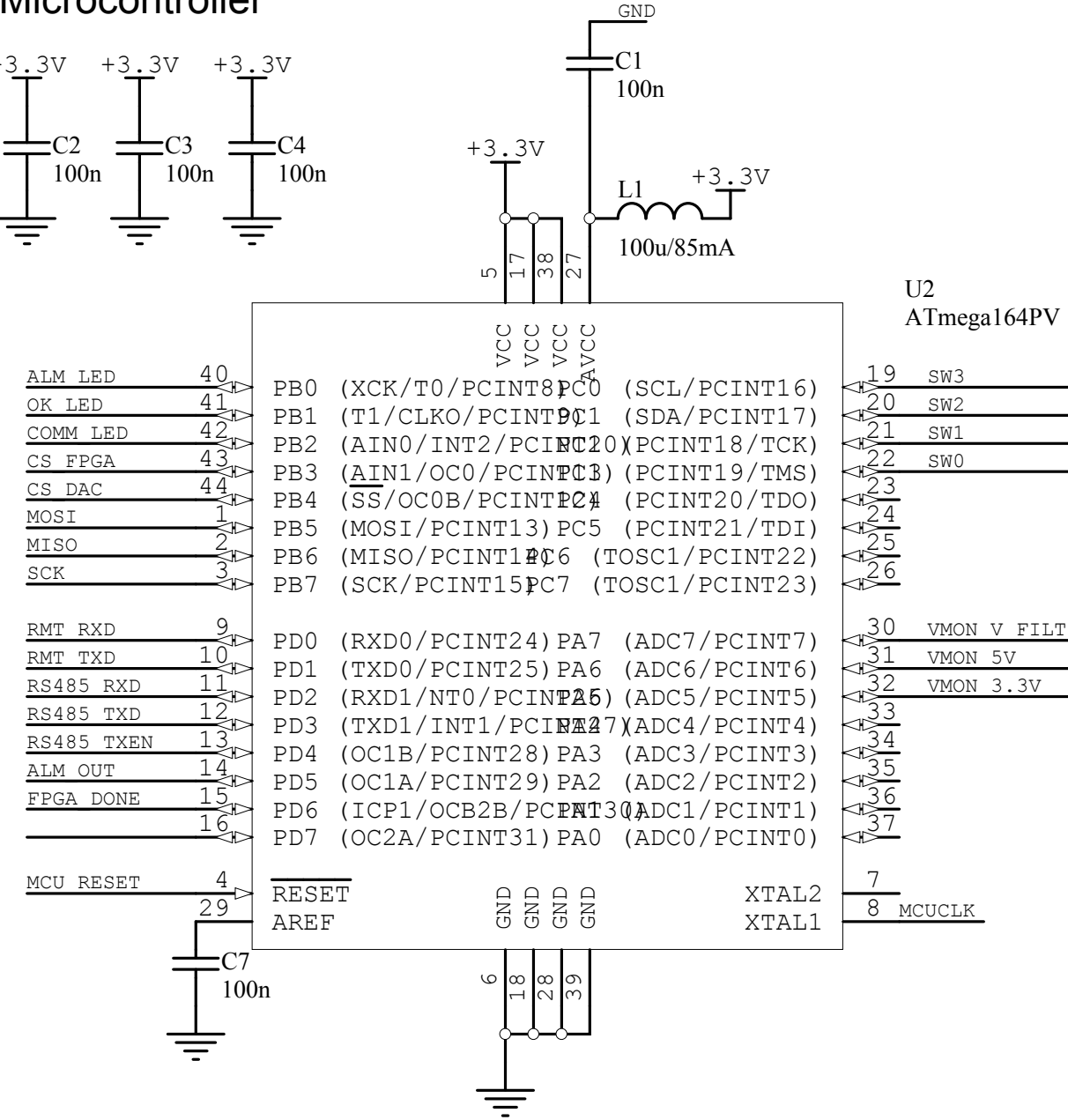
Do not populate:
U18-21, C39-42, J13, J14

PARIO - With Parallel I/O

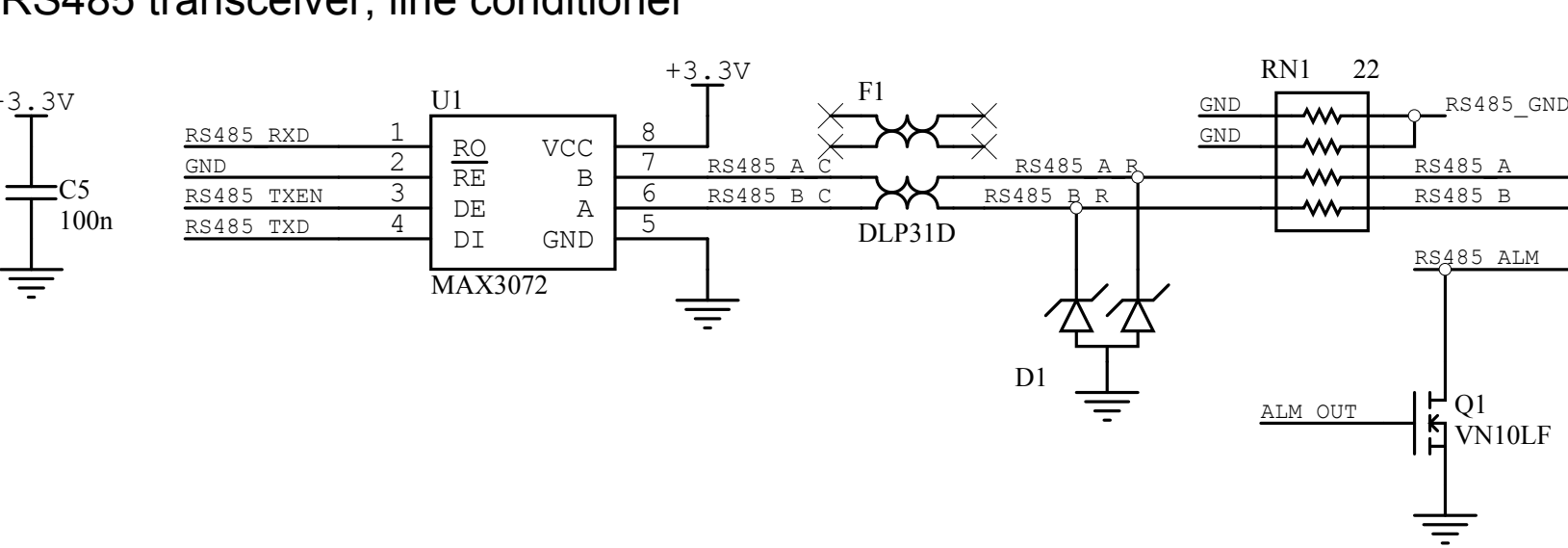
Do not populate:

The default configuration is NOUMAC, NOPAR

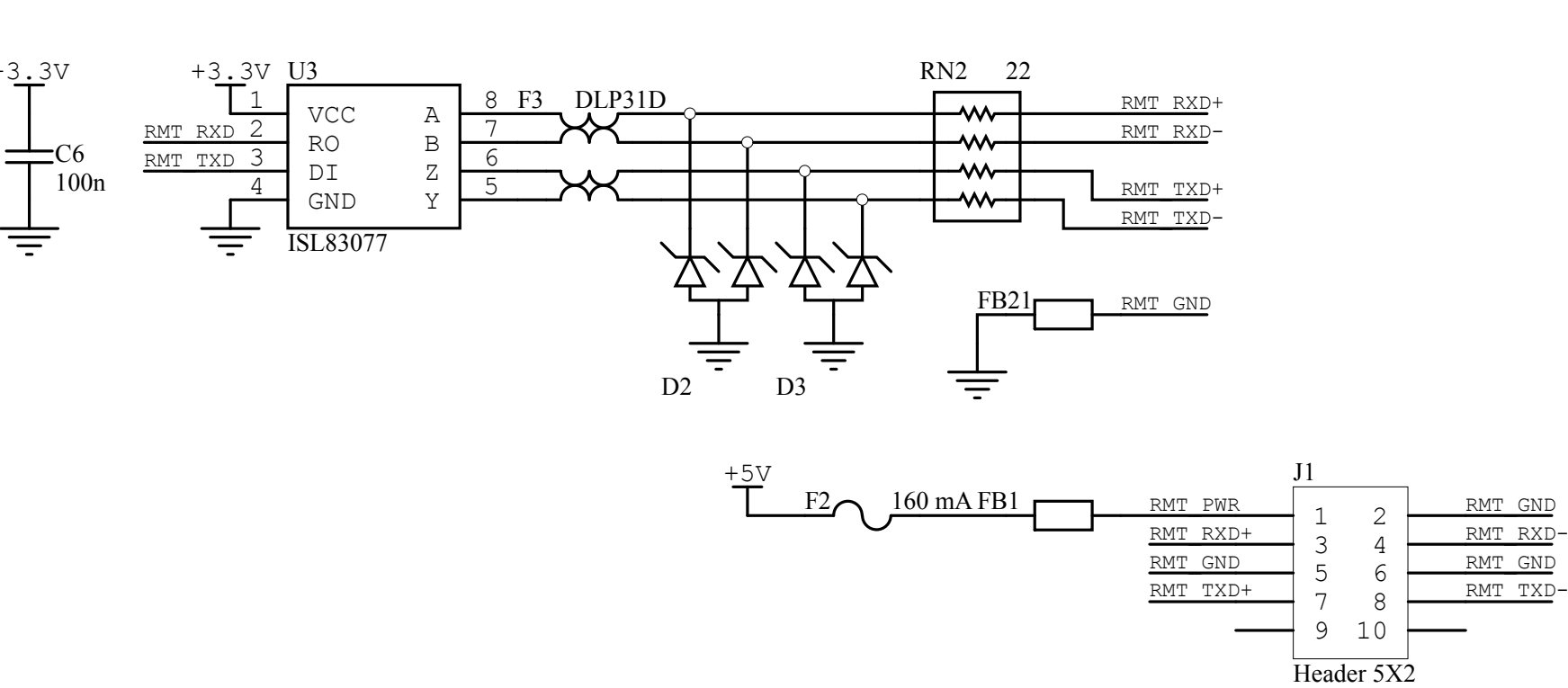
Microcontroller



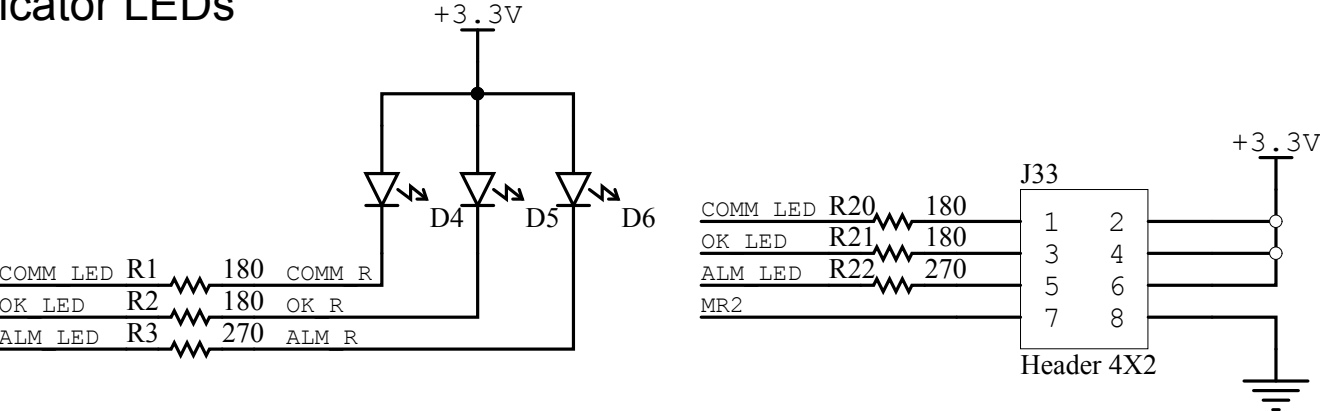
RS485 transceiver, line conditioner



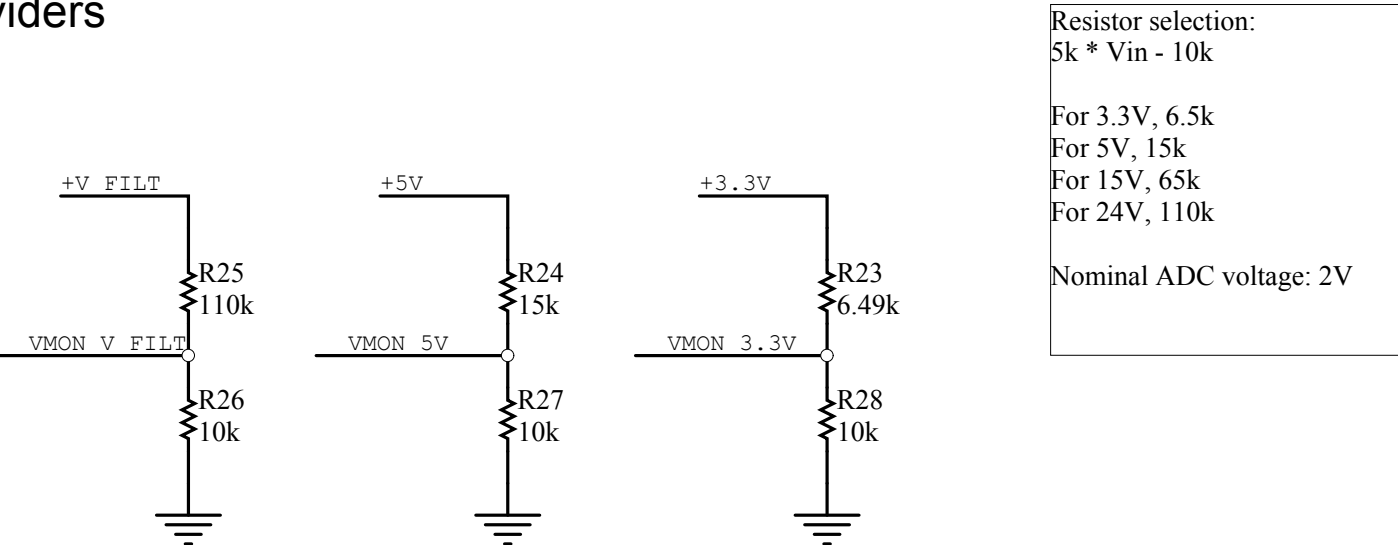
Remote Controller Link



Indicator LEDs



Voltage Monitor dividers

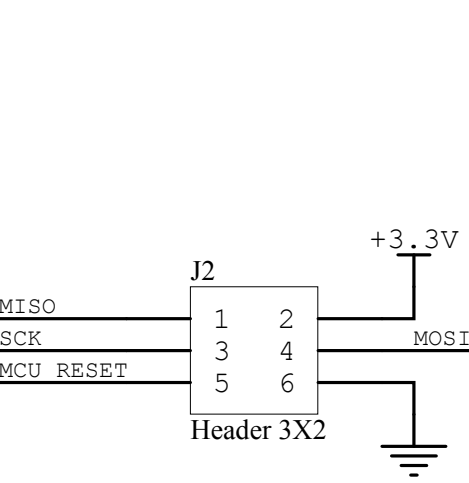


Resistor selection:
5k * Vin - 10k

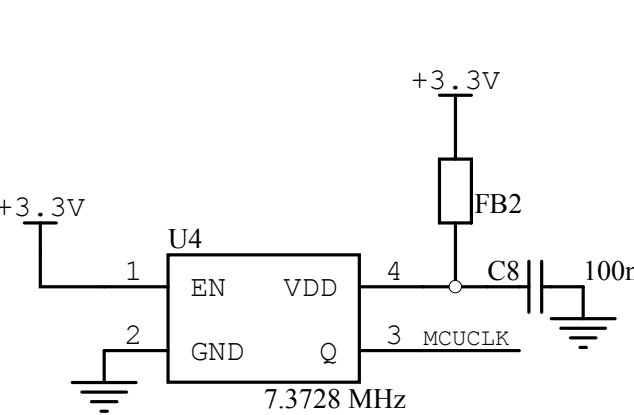
For 3.3V, 6.5k
For 5V, 15k
For 15V, 65k
For 24V, 110k

Nominal ADC voltage: 2V

Prog. Connector

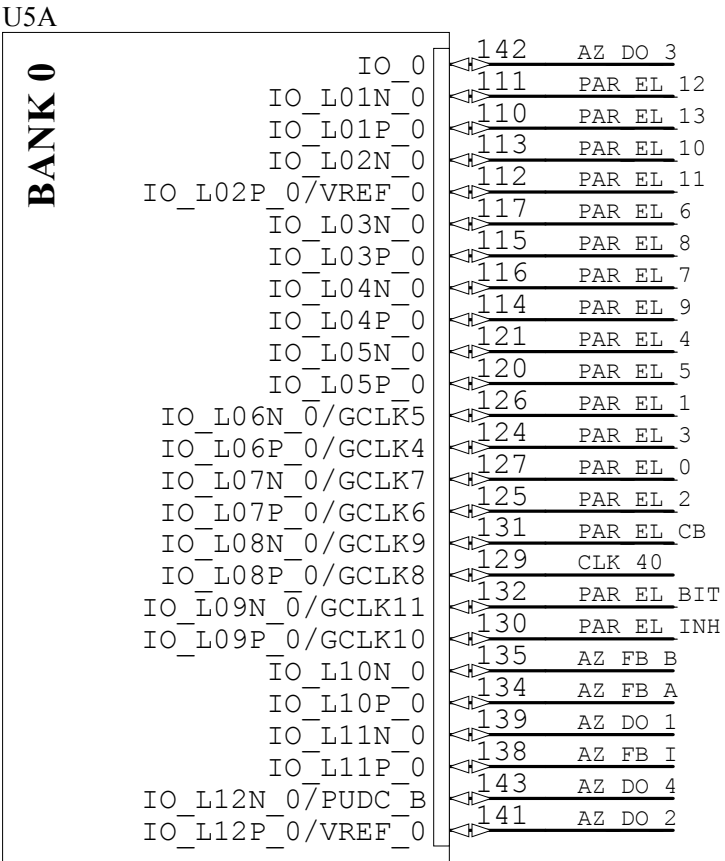


MCU Clock

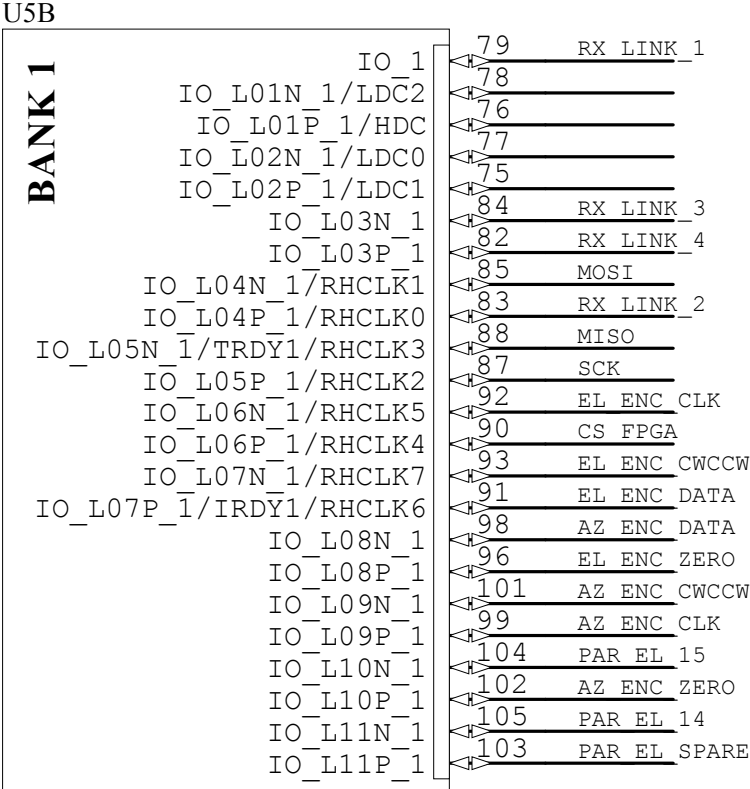


Title <i>Pedestal Interface - Microcontroller</i>			CSU-CHILL 30750 Weld County Road 45 Greeley, CO 80631	Engineer: JG
Size: Letter	Number: wibex_pi_2	Revision: 1.1		Drawn By: JG
Date: 5/28/2009	Time: 9:25:34 AM	Sheet 2 of 8		
File: C:\Documents and Settings\jgeorge\My Documents\pcb\angleconvert\ac_mcu.SchDoc				
			Colorado State University	

FPGA I/O

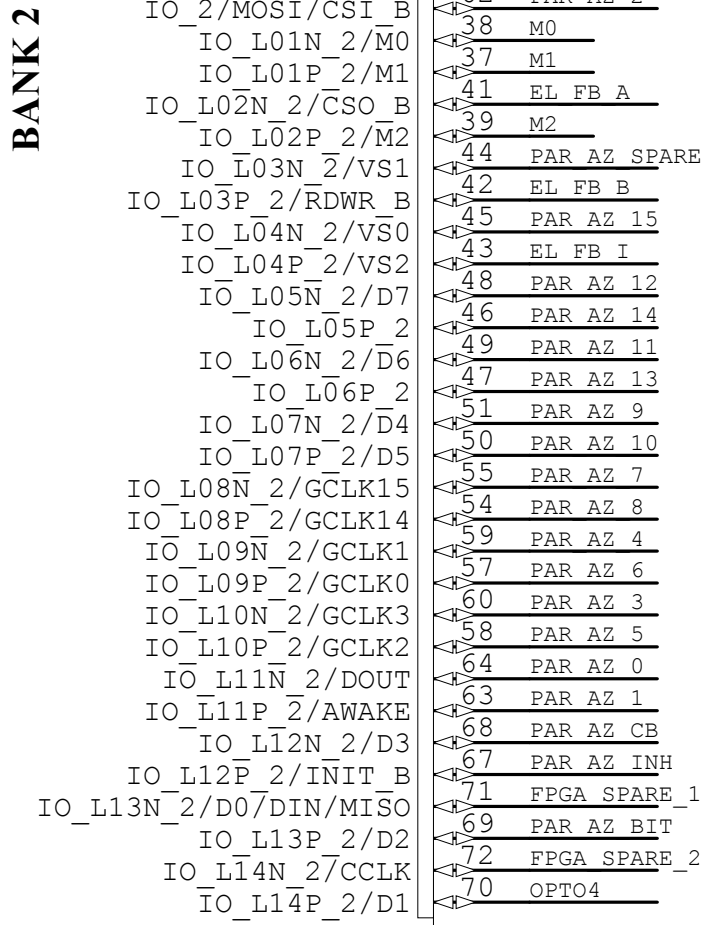


XC3S50AN-4TQ144I



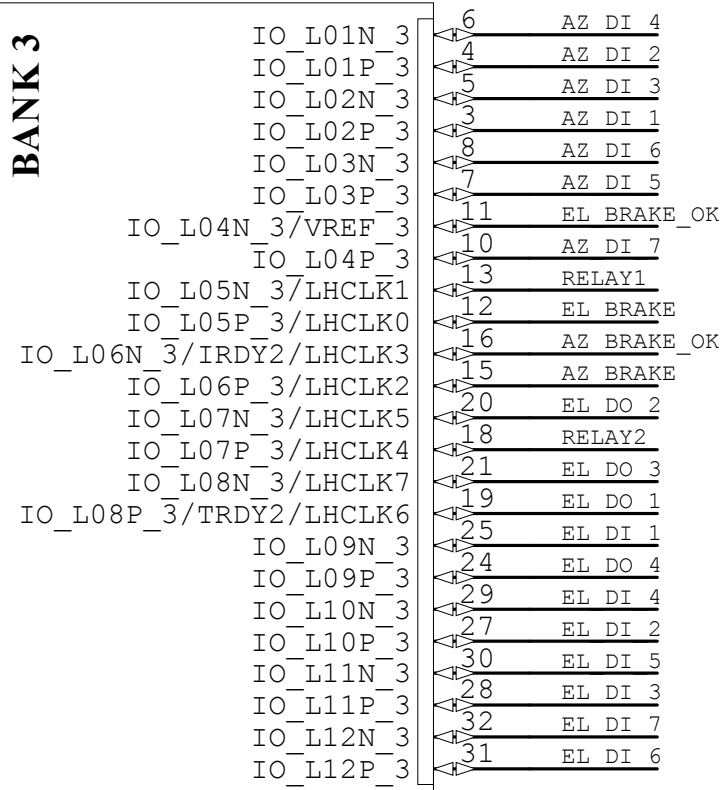
XC3S50AN-4TQ144I

U5C

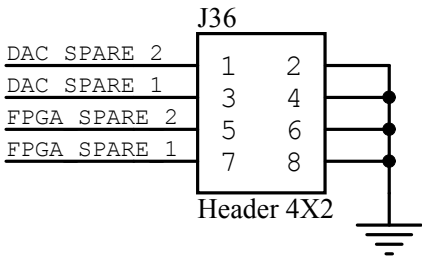


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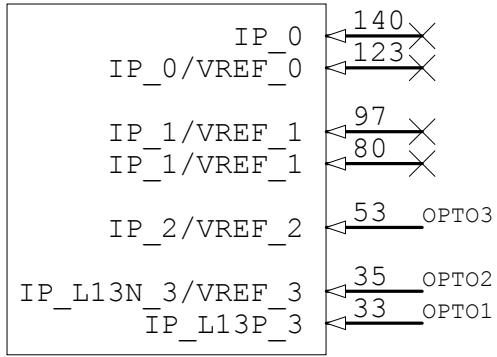
U5D



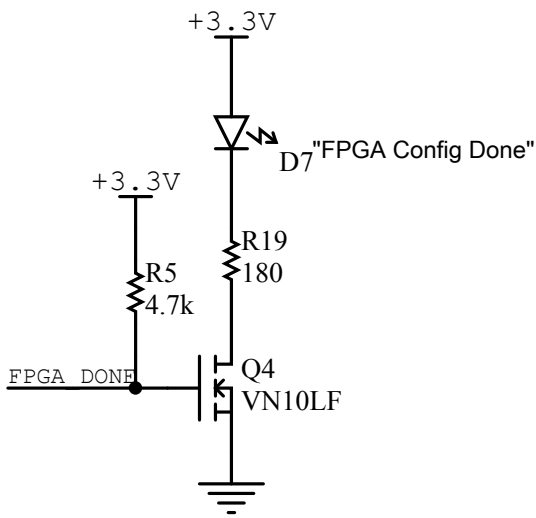
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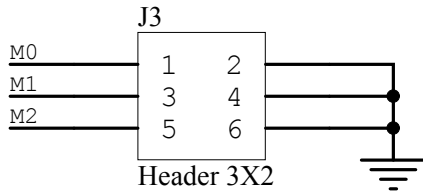
U5E



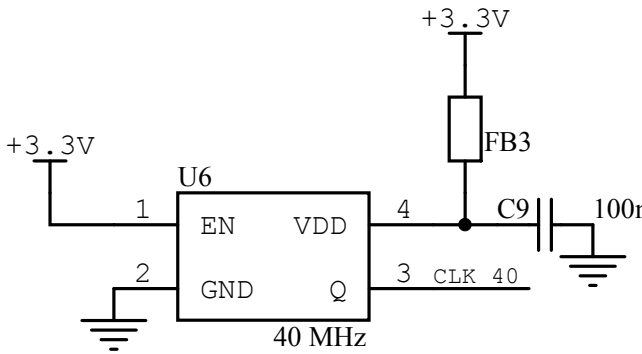
XC3S50AN-4TQ144I



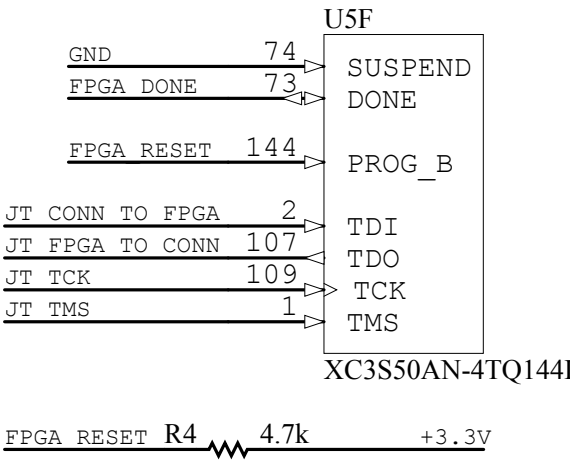
Config Mode



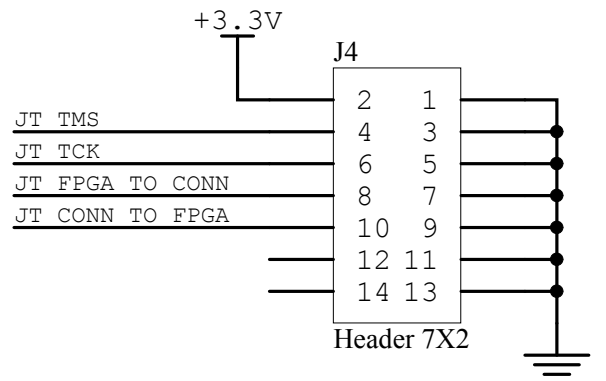
FPGA Clock



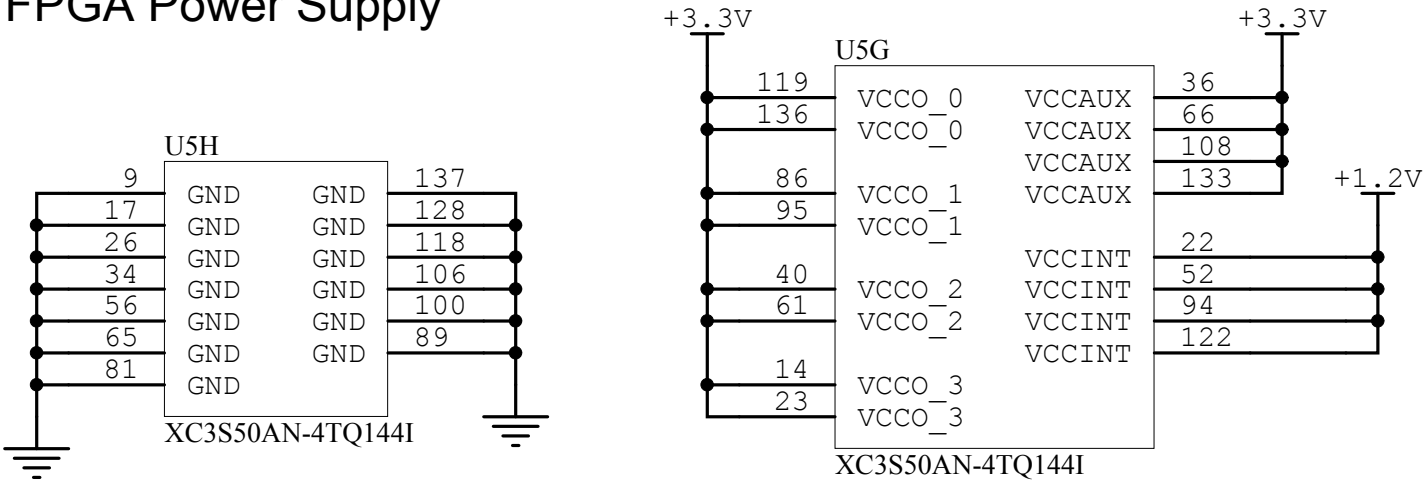
FPGA Configuration Interface



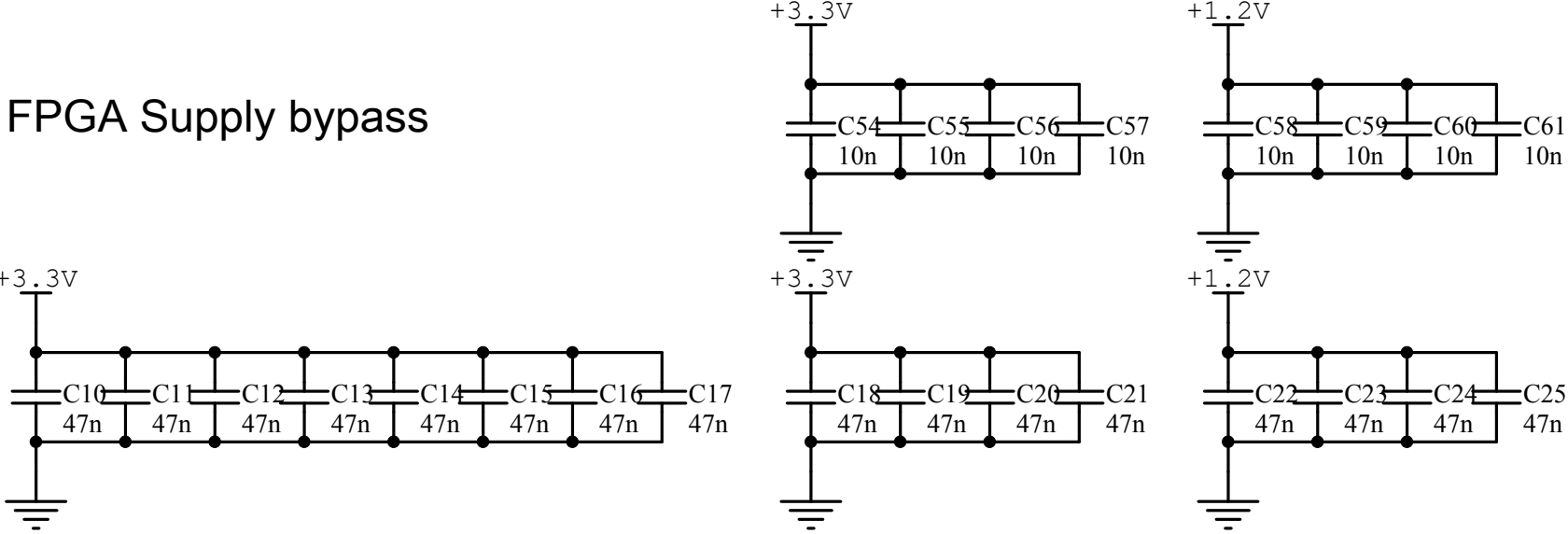
FPGA JTAG Port



FPGA Power Supply



FPGA Supply bypass



Title **Pedestal Interface - FPGA**

CSU-CHILL
30750 Weld County Road 45
Greeley, CO 80631

Engineer:
JG

Size: Letter

Number: wibex_pi_3

Revision: 1.1

Date: 5/28/2009

Time: 9:25:34 AM

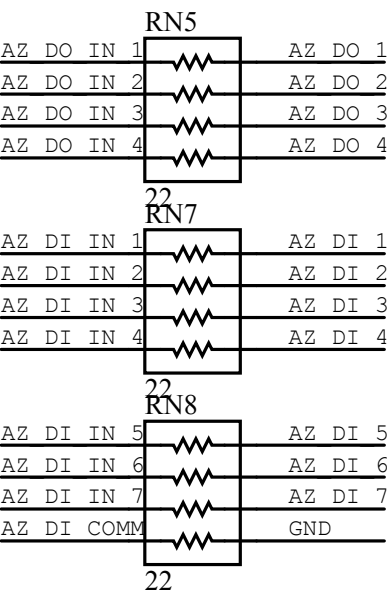
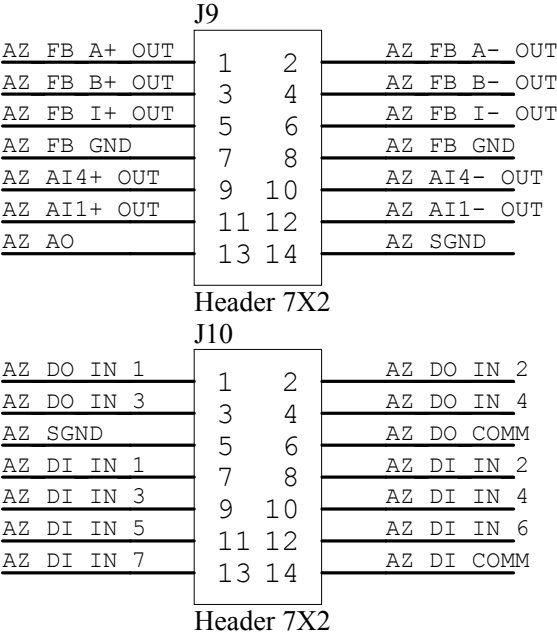
Sheet 3 of 8

Colorado State University

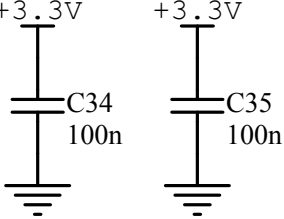
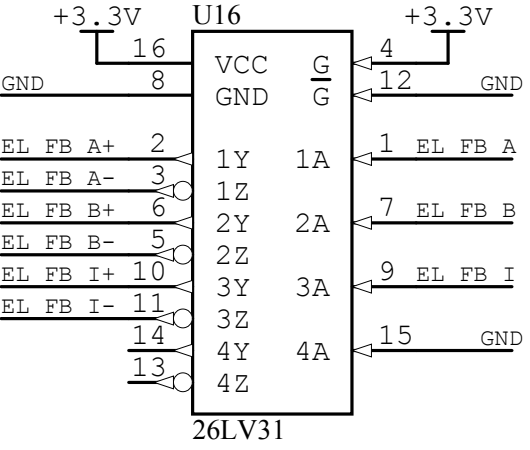
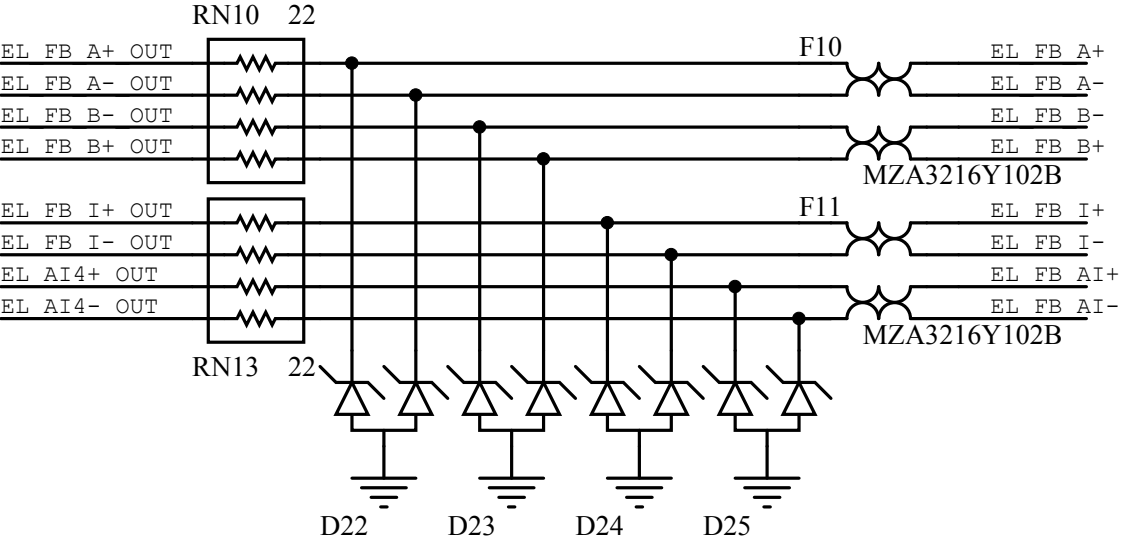
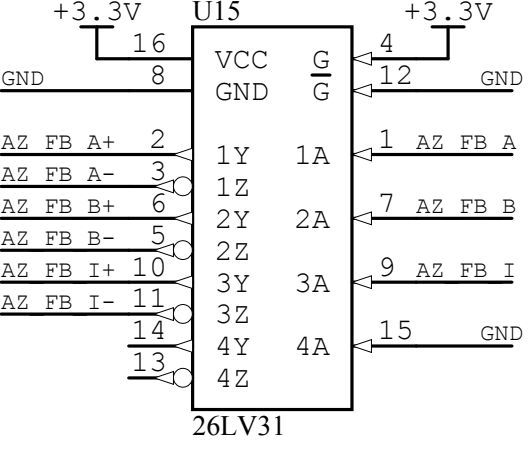
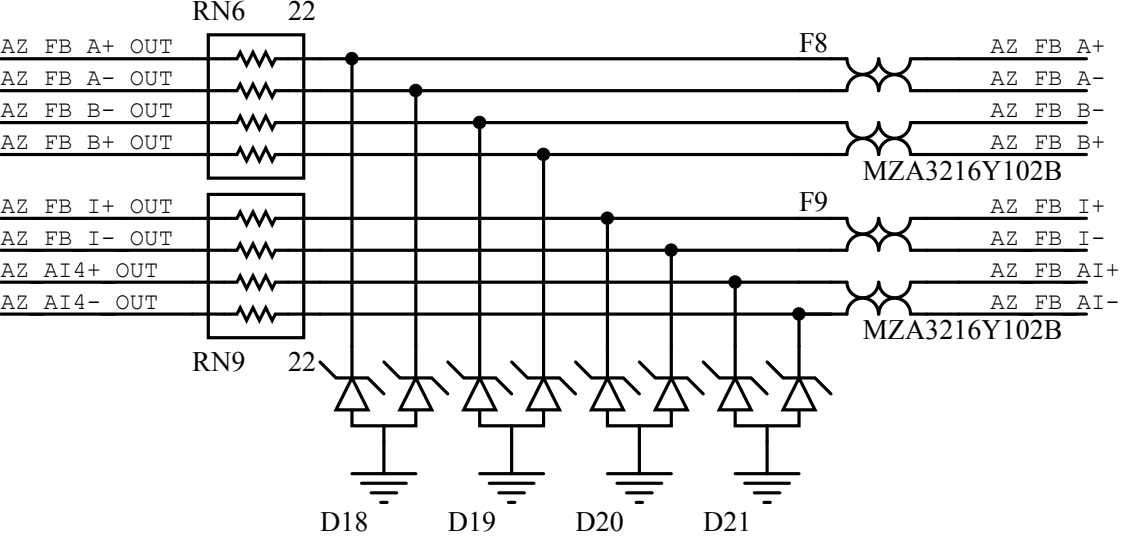
Drawn By:
JG

File: C:\Documents and Settings\jgeorge\My Documents\pcb\angleconvert\ac_fpga.SchDoc

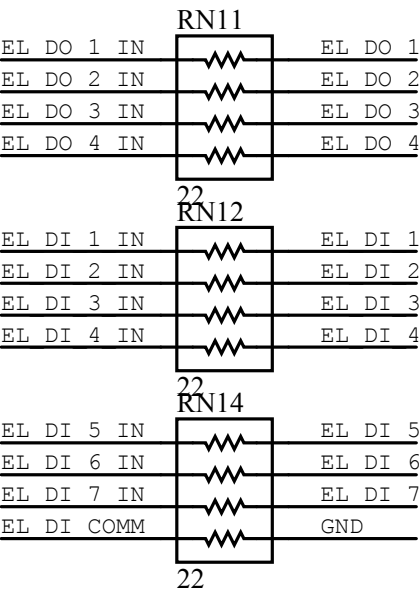
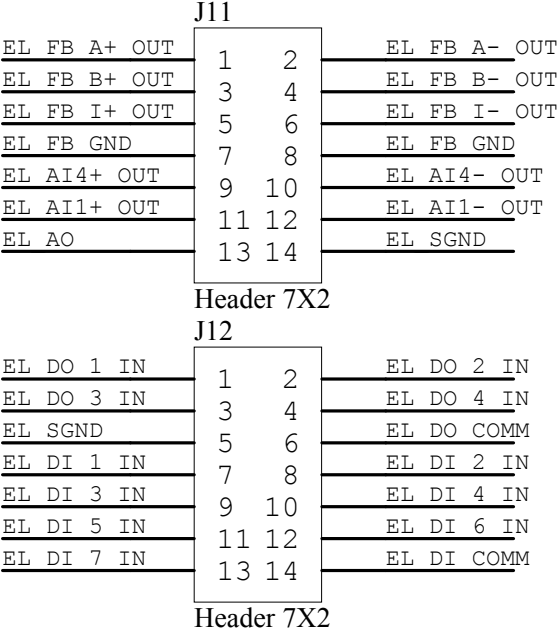
Azimuth Digital I/O Connector



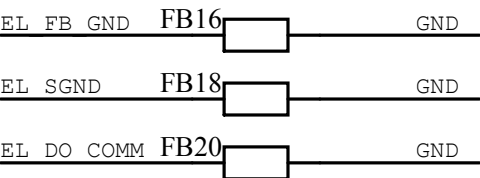
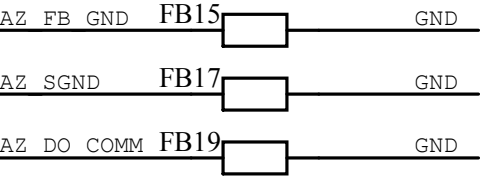
Simulated Incremental Encoder output drivers, protection network



Elevation Digital I/O Connector



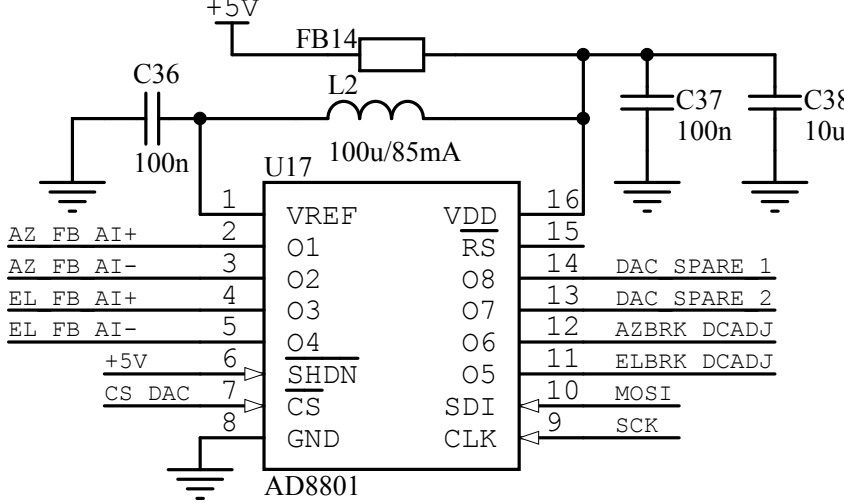
Digital I/O Grounding



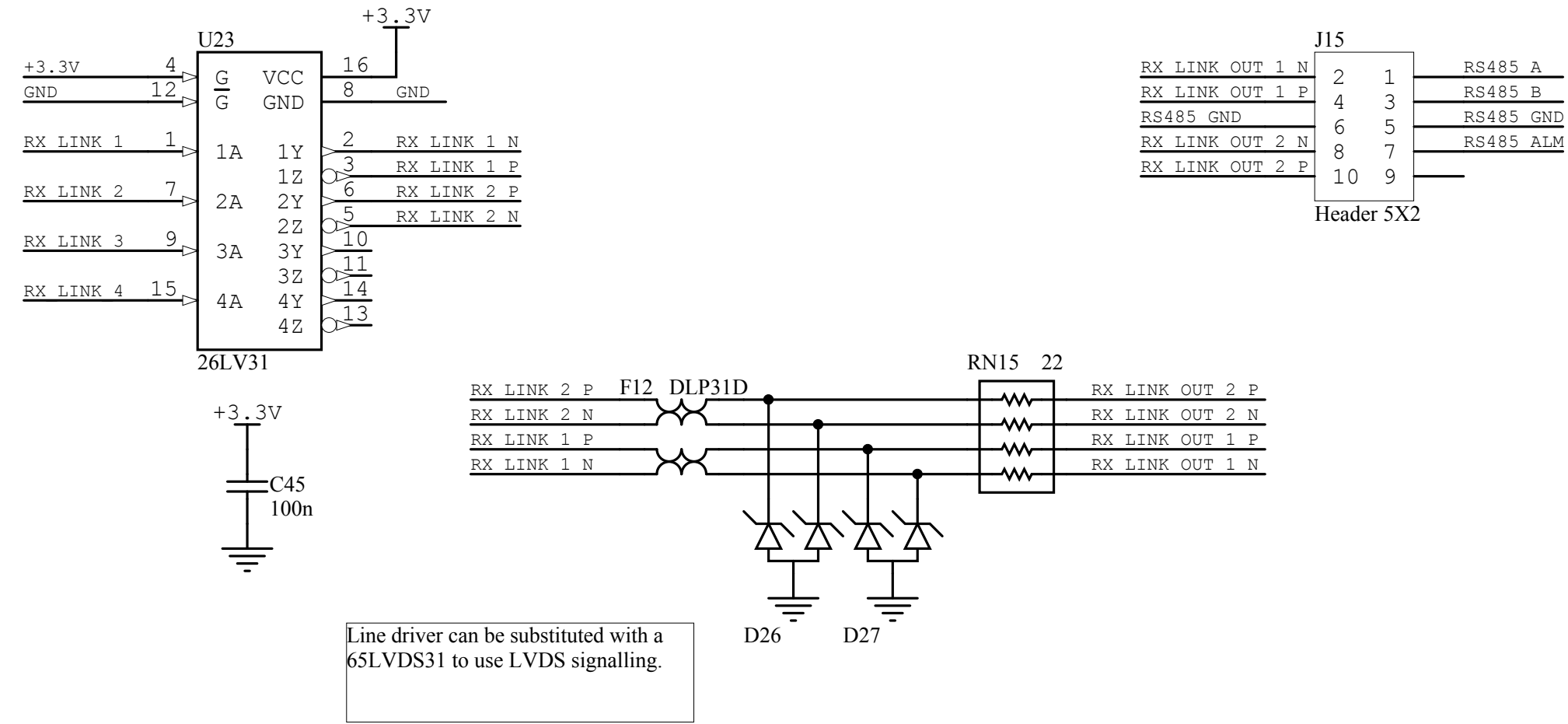
DAC

The DAC controls the Az and El Analog Inputs differentially (software writes different values to each channel pair)

Also, the duty cycle control for the brake drivers are controlled by output channels 5 and 6

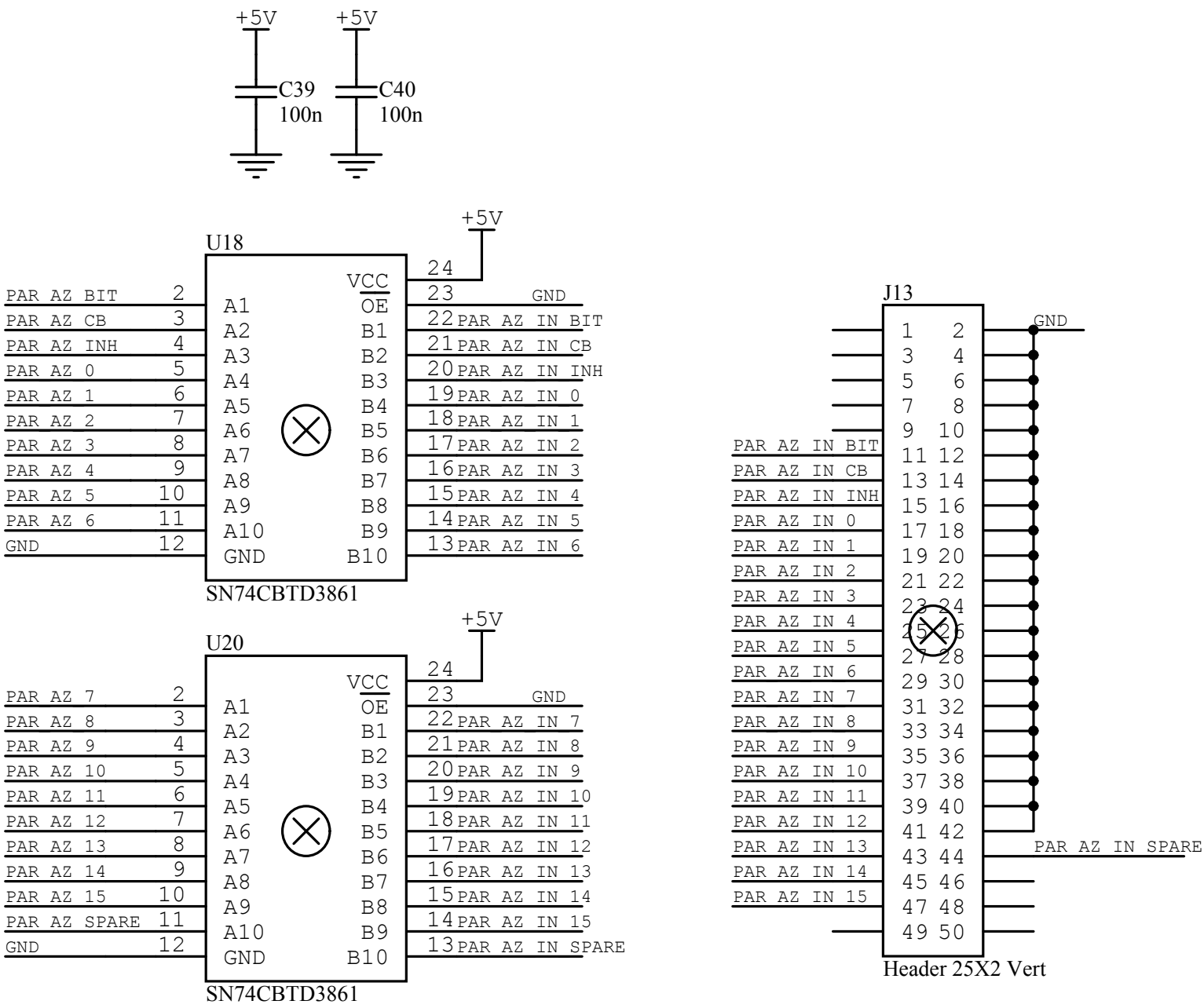


Digital Receiver Link

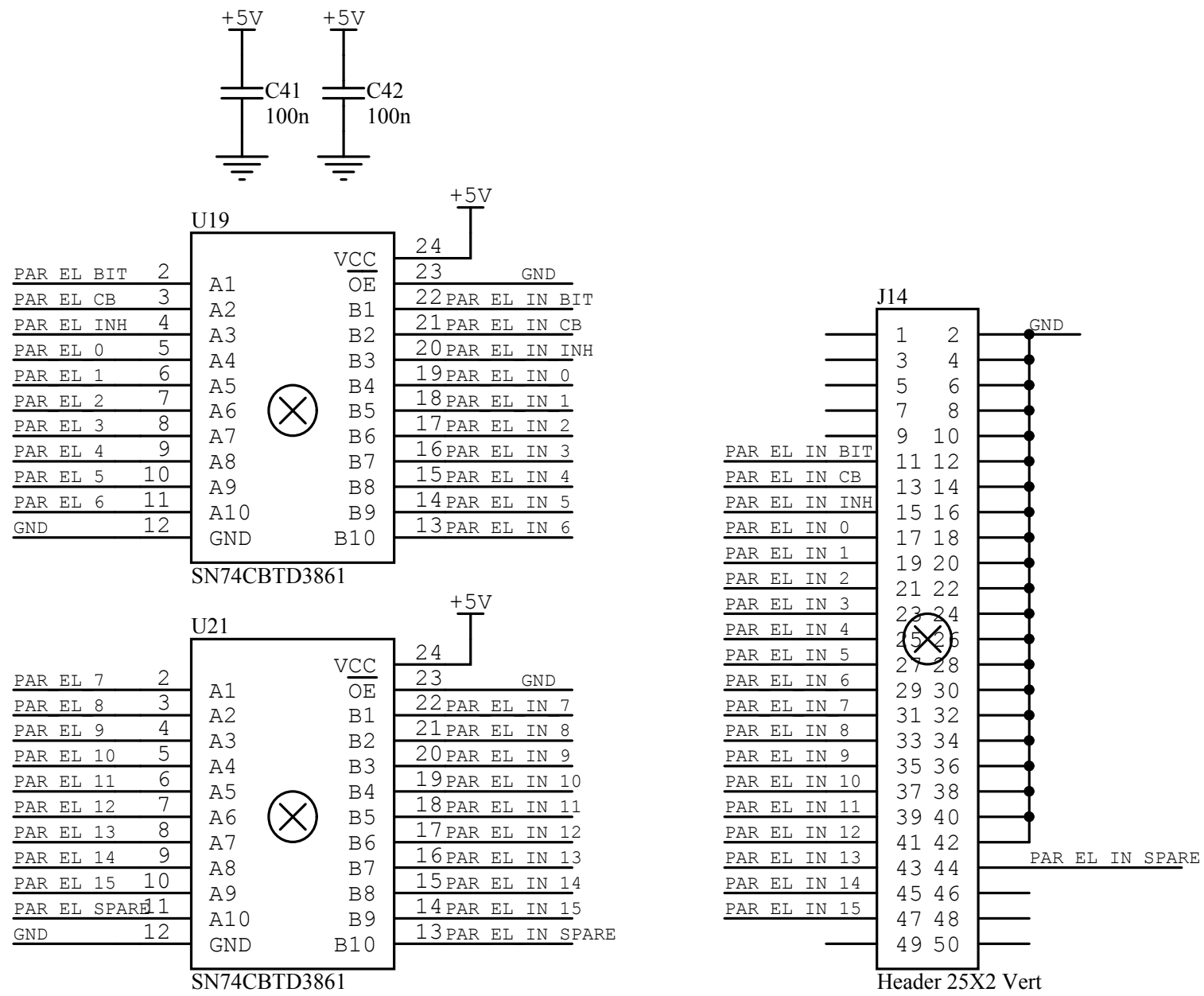


Fiber Optic Angle Link

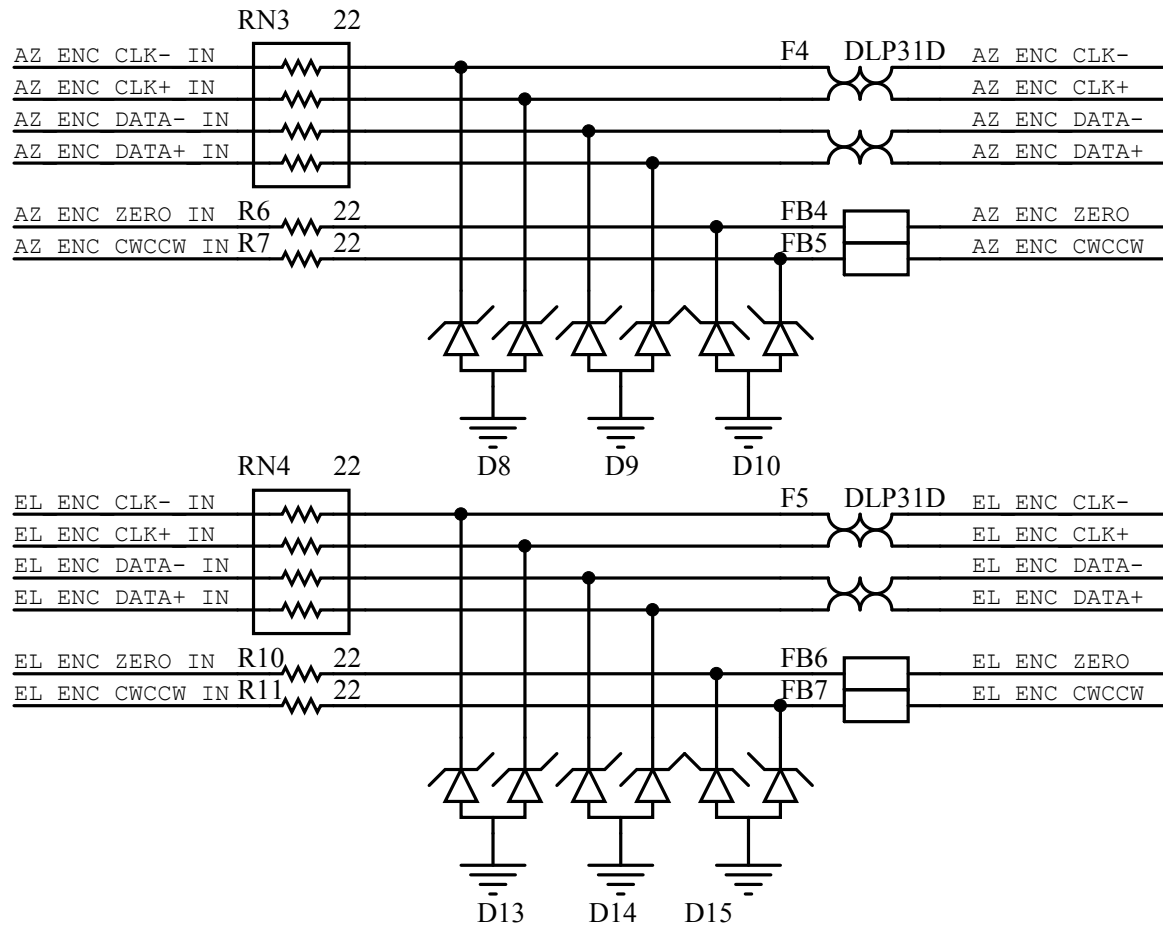
Parallel Angle Input - Azimuth



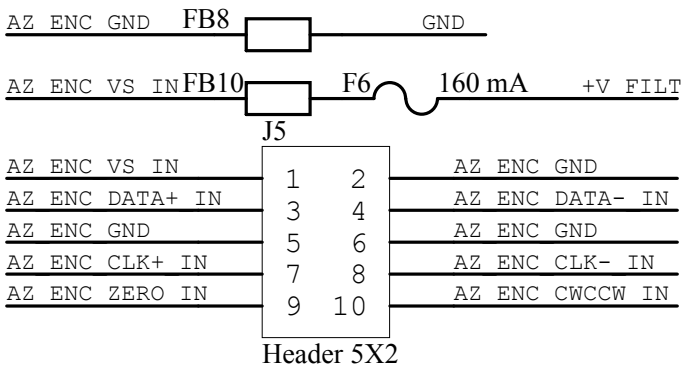
Parallel Angle Input - Elevation



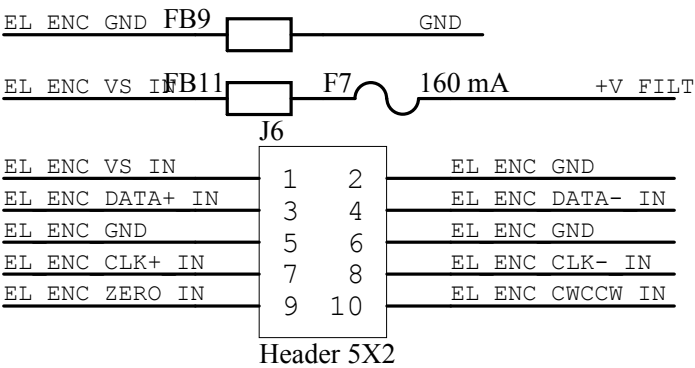
Encoder I/O Protection Network



Azimuth Encoder Connector



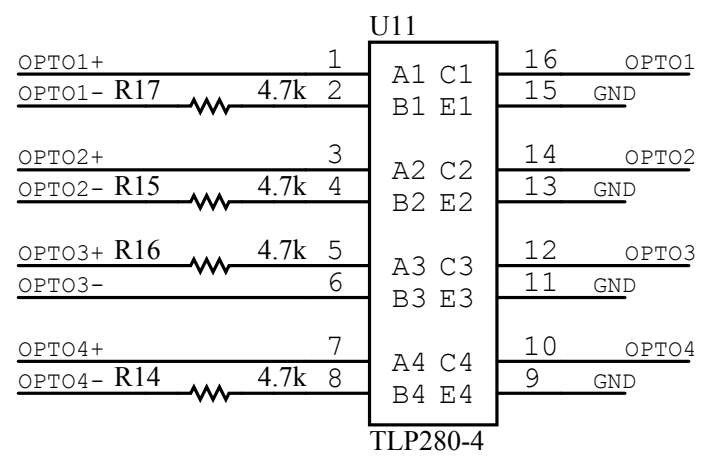
Elevation Encoder Connector



Common I/O, Brake connector



Isolated Digital Inputs

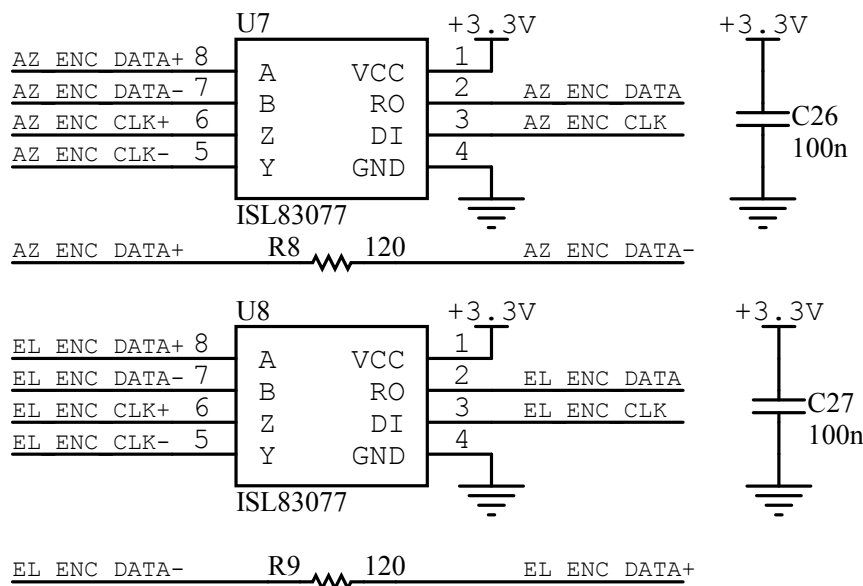


Series resistor values may be changed depending on input voltage range. Optoisolator forward current is 5mA.

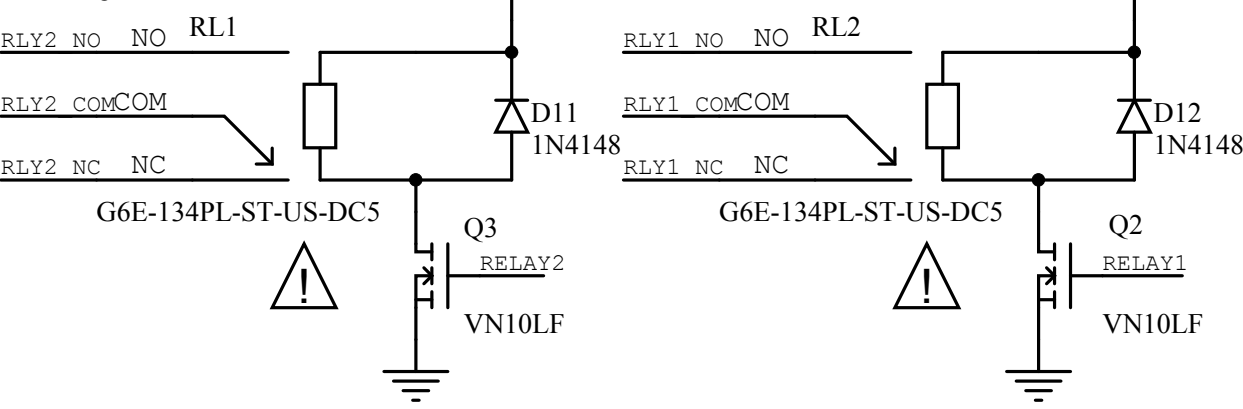
Note: Optoisolators are bidirectional

5V -> 200
24V -> 4.7k
120V -> 24k

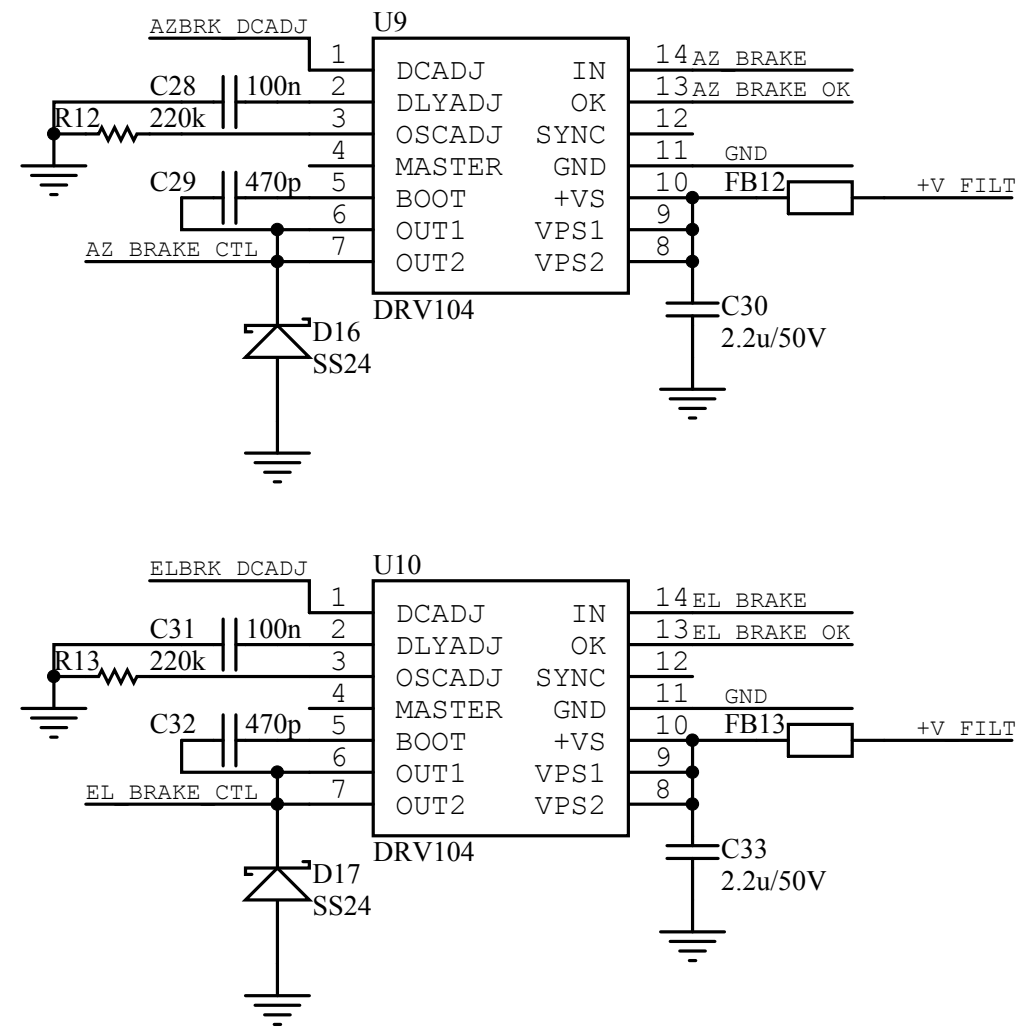
SSI Encoder Driver/Receiver



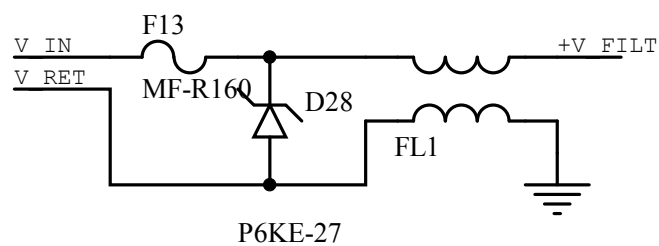
Relay, Drivers



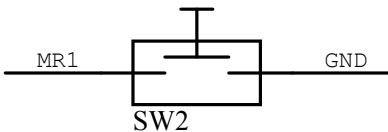
Brake Control



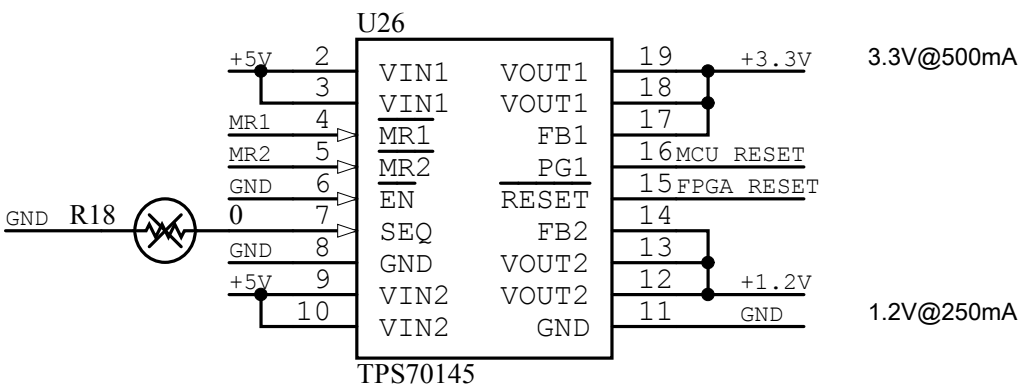
Power Entry, Protection



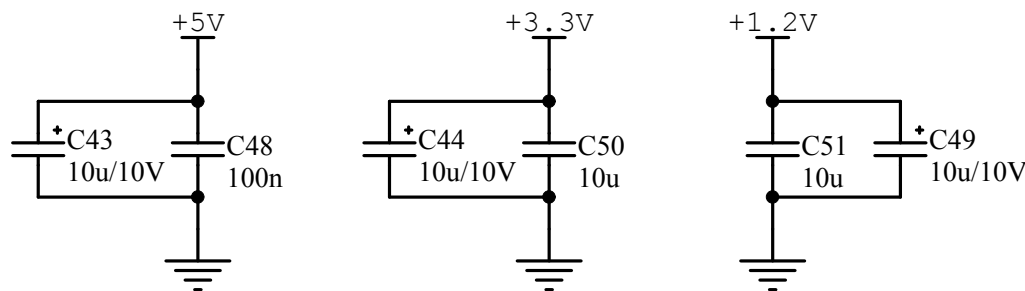
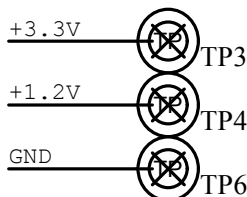
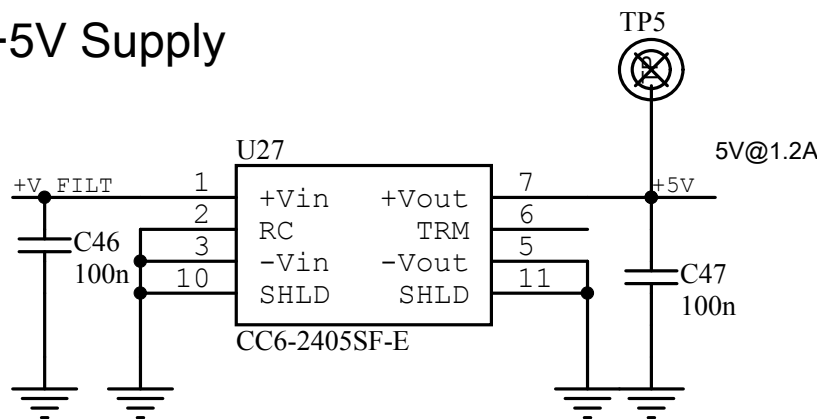
Manual Reset



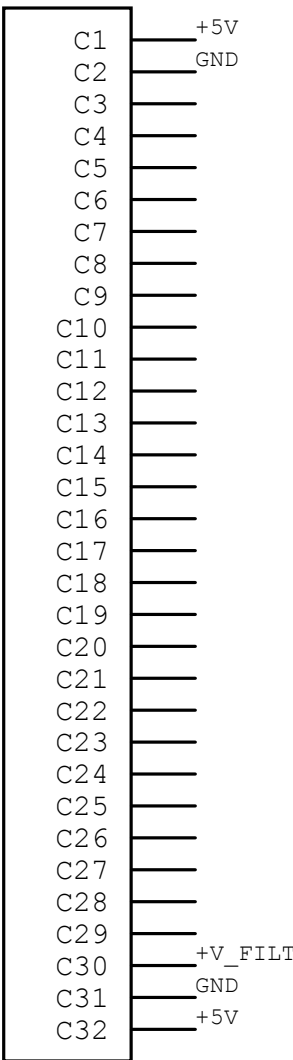
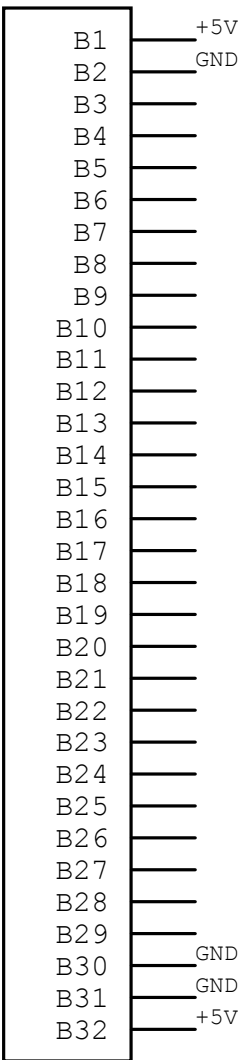
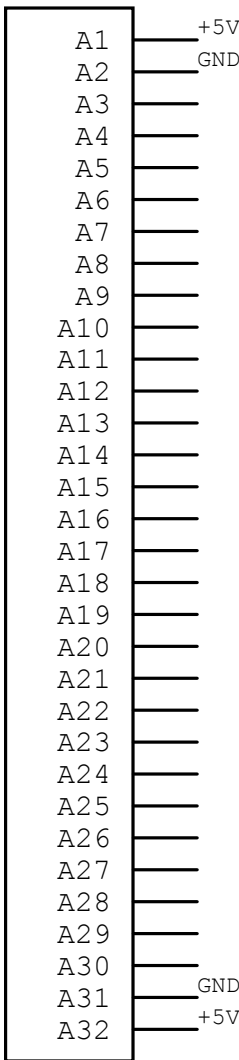
FPGA Supplies



+5V Supply



UMAC Chassis connector



Title <i>Pedestal Interface - Power Supplies</i>			CSU-CHILL 30750 Weld County Road 45 Greeley, CO 80631	Engineer: JG
Size: Letter	Number: wibex_pi_8	Revision: 1.1		Drawn By: JG
Date: 5/28/2009	Time: 9:25:35 AM	Sheet 8 of 8		
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